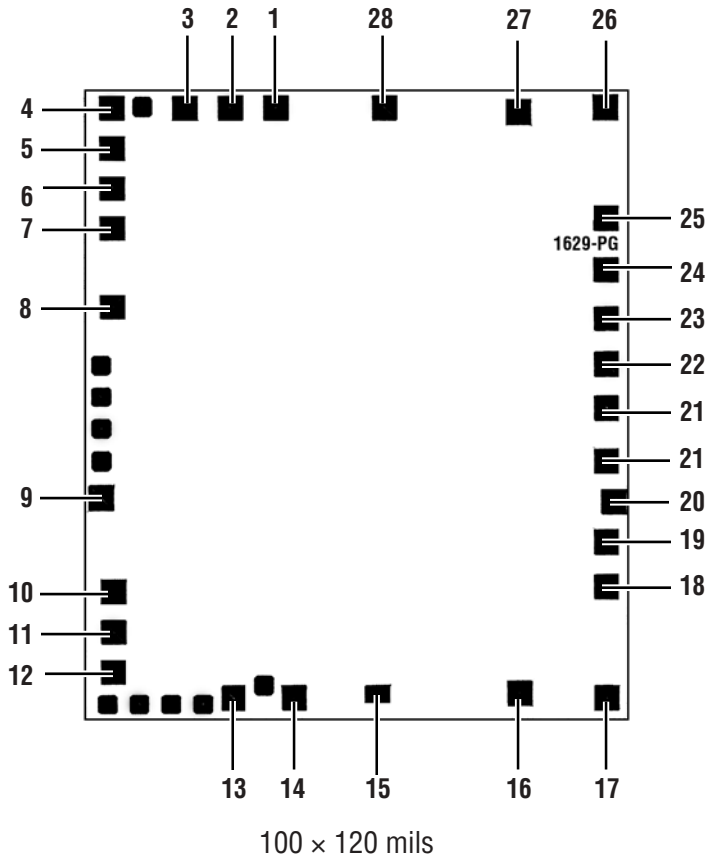


**Polyphase, High Efficiency, Synchronous
 Step-Down Switching Regulator**
DIE CROSS REFERENCE

LTC Finished Part Number	Order DICE CANDIDATE Part Number Below
LTC1629-PG LTC1629-PG	LTC1629-PG DICE LTC1629-PG DWF

PAD FUNCTION

1. RUN/SS	15. PGOOD
2. SENSE1 ⁺	16. TG2
3. SENSE1 ⁻	17. SW2
4. EAIN	18. BOOST2
5. PLLFLTR	19. BG2
6. PLLIN	20. PGND
7. PHASMD	21. INTV _{CC}
8. I _{TH}	22. EXTV _{CC}
9. SGND	23. BG1
10. V _{DIFFOUT}	24. V _{IN}
11. V _{OS} ⁻	25. BOOST1
12. V _{OS} ⁺	26. SW1
13. SENSE2 ⁻	27. TG1
14. SENSE2 ⁺	28. CLKOUT


DICE ELECTRICAL TEST LIMITS
 $T_A = 25^\circ\text{C}$, $V_{IN} = 15\text{V}$, $V_{RUN/SS} = 5\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
Main Control Loop					
V_{EAIN}	Regulated Feedback Voltage	(Note 1); I_{TH} Voltage = 1.2V	0.792	0.808	V
$V_{SENSEMAX}$	Maximum Current Sense Threshold	$V_{SENSE1, 2} = 5\text{V}$;	65	85	mV
I_{INEAIN}	Feedback Current	(Note 1)		-50	nA
$V_{LOADREG}$	Output Voltage Load Regulation	(Note 1)			
		Measured in Servo Loop; I_{TH} Voltage = 0.7V		0.5	%
		Measured in Servo Loop; I_{TH} Voltage = 2V		-0.5	%
$V_{REFLNREG}$	Reference Voltage Line Regulation	$V_{IN} = 3.6\text{V}$ to 30V (Note 1)		0.02	%/V
V_{OVL}	Output Overvoltage Threshold	Measured at V_{EAIN}	0.84	0.88	V
UVLO	Undervoltage Lockout	V_{IN} Ramping Down	3	4	V
I_Q	Input DC Supply Current Shutdown	(Note 4); $V_{RUN/SS} = 0\text{V}$		40	μA
$I_{RUN/SS}$	Soft-Start Charge Current	$V_{RUN/SS} = 1.9\text{V}$	-0.5		μA

DICE/DFN SPECIFICATION

LTC1629-PG

DICE ELECTRICAL TEST LIMITS

$T_A = 25^\circ\text{C}$. $V_{IN} = 15\text{V}$, $V_{RUN/SS} = 5\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
$V_{RUN/SS}$	RUN/SS Pin ON Threshold	$V_{RUN/SS}$ Rising	1.0	1.9	V
$V_{RUN/SSLO}$	RUN/SS Pin Latchoff Arming	$V_{RUN/SS}$ Rising from 3V		4.5	V
I_{SCL}	RUN/SS Discharge Current	Soft Short Condition $V_{EAIN} = 0.5\text{V}$; $V_{RUN/SS} = 4.5\text{V}$	0.5	4	μA
I_{SDLDO}	Shutdown Latch Disable Current	$V_{EAIN} = 0.5\text{V}$		5	μA
I_{SENSE}	Total Sense Pins Source Current	Each Channel; $V_{SENSE1-}, 2- = V_{SENSE1+}, 2+ = 0\text{V}$	-85		μA
DF_{MAX}	Maximum Duty Factor	In Dropout	98		%
$TG1, 2 t_r$ $TG1, 2 t_f$	Top Gate Transition Time:				
	Rise Time	$C_{LOAD} = 3300\text{pF}$		90	ns
	Fall Time	$C_{LOAD} = 3300\text{pF}$		90	ns
$BG1, 2 t_r$ $BG1, 2 t_f$	Bottom Gate Transition Time:				
	Rise Time	$C_{LOAD} = 3300\text{pF}$		90	ns
	Fall Time	$C_{LOAD} = 3300\text{pF}$		90	ns
Internal V_{CC} Regulator					
V_{INTVCC}	Internal V_{CC} Voltage	$6\text{V} < V_{IN} < 30\text{V}$; $V_{EXTVCC} = 4\text{V}$	4.8	5.2	V
$V_{LDO INT}$	INT V_{CC} Load Regulation	$I_{CC} = 0$ to 20mA; $V_{EXTVCC} = 4\text{V}$		1.0	%
$V_{LDO EXT}$	EXT V_{CC} Voltage Drop	$I_{CC} = 20\text{mA}$; $V_{EXTVCC} = 5\text{V}$;		240	mV
V_{EXTVCC}	EXT V_{CC} Switchover Voltage	$I_{CC} = 20\text{mA}$, EXT V_{CC} Ramping Positive	4.5		V
Oscillator and Phase-Locked Loop					
f_{NOM}	Nominal Frequency	$V_{PLLFLTR} = 1.2\text{V}$	190	250	kHz
f_{LOW}	Lowest Frequency	$V_{PLLFLTR} = 0\text{V}$	120	160	kHz
f_{HIGH}	Highest Frequency	$V_{PLLFLTR} \geq 2.4\text{V}$	280	360	kHz
R_{RELPHS}	Controller 2-Controller 1 Phase	$V_{PHASMD} = 0\text{V}$, Open $V_{PHASMD} = 5\text{V}$		180 240	Deg Deg
CLKOUT	Phase (Relative to Controller 1)	$V_{PHASMD} = 0\text{V}$ $V_{PHASMD} = \text{Open}$ $V_{PHASMD} = 5\text{V}$		60 90 120	Deg Deg Deg
CLK _{HIGH}	Clock High Output Voltage		4		V
CLK _{LOW}	Clock Low Output Voltage			0.2	V
Differential Amplifier/Op Amp Gain Block					
A_{DA}	Gain	Differential Amp Mode	0.995	1.005	V/V
CMRR _{DA}	Common Mode Rejection Ratio	Differential Amp Mode; $0\text{V} < V_{CM} < 5\text{V}$	46		dB
PGOOD Output					
V_{PGL}	PGOOD Voltage Low	$I_{PGOOD} = 2\text{mA}$		0.3	V
I_{PGOOD}	PGOOD Leakage Current	$V_{PGOOD} = 5\text{V}$		± 1	μA
V_{PG}	PGOOD Trip Level, Either Controller	V_{EAIN} with Respect to Set Output Voltage V_{EAIN} Ramping Negative V_{EAIN} Ramping Positive	-6 6	-9.5 9.5	% %

Note 1: The LTC1629-PG is tested in a feedback loop that serves V_{ITH} to a specified voltage and measures the resultant V_{EAIN} .

Wafer level testing is performed per the indicated specifications for dice. Considerable differences in performance can often be observed for dice versus packaged units due to the influences of packaging and assembly on certain devices and/or parameters. Please consult factory for more information on dice performance and lot qualifications via lot sampling test procedures.

Dice data sheet subject to change. Please consult factory for current revision in production.

I.D.No. 66-13-1351

2

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LT/LT 0405 PRINTED IN USA



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